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Design of Resource Efficient Low Power Correlator for Communication

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Abstract-This paper deals with the timing synchronization resource utilization and power consumption problems of OFDM .Nowadays multiplier based correlators are used in OFDM systems. It occupies large areas making it tough to fit in VLSI devices. Hence in this project we proposed a new technique which uses multiplierless correlators in OFDM systems .Multiplierless correlators based on multiple constant multiplication technique for area reduction is used in modified correlator. These correlators can fit on low power VLSI devices thus resource utilization can be done effectively. Comparison of multiplier based correlator and multiple constant multiplications by using carry look ahead adder and carry select adder correlator gives the clear understanding of area overhead problem. Thus multiplierless correlators provide accurate timing synchronization even at high clock speeds. Thus simulated output generator using MODELSIM and Xilinx shows that the OFDM using multiplierless correlators gives better timing synchronization than OFDM using multiplier based correlators. .

Index Terms- FPGA, OFDM, Correlator**,** Cyclic Prefix.

1. INTRODUCTION

Orthogonal frequency division multiplexing (OFDM) is a multicarrier modulation technique that has used for wireless communication systems due to the high spectral efficiency, immunity to multipath distortion, and being flexible to integrate with other techniques. However, the high-peak-to-average power ratio and sensitivity to synchronization errors are the major drawbacks for OFDM systems. The algorithms and architectures for symbol timing and frequency synchronization have been addressed in this thesis because of their critical requirements in the development and implementation of wireless OFDM systems. For the frequency synchronization, two efficient carrier frequency offset (CFO) estimation methods based on the power and phase difference measurements between the subcarriers in consecutive OFDM symbols have been presented and the power difference measurement technique is mapped onto reconfigurable hardware architecture.

The performance of the considered CFO estimators is investigated in the presence of timing uncertainty conditions. The power difference measurements approach is further investigated for timing synchronization in OFDM systems with constant modulus constellation. A new symbol timing estimator has been proposed by measuring the power difference either between adjacent subcarriers or the same subcarrier in consecutive OFDM symbols. The proposed timing metric has been realized in feed forward and feedback configurations, and different implementation strategies have been considered to enhance the performance and reduce the complexity.

Recently, Multiple-Input Multiple-Output (MIMO) wireless communication systems have received considerable attention. Therefore, the proposed algorithms have also been extended for timing recovery and frequency synchronization in MIMO-OFDM systems. Orthogonal frequency division multiplexing (OFDM) is an effective modulation technique is simply defined as modulating a signal with multiple subcarrier frequencies. It is used in both wired and wireless communication systems. The advantages of spectral efficiency and robustness to multipath fading, OFDM was specified for multiple applications in high bit-rate wireless transmission systems such as wireless local area networks adopted by IEEE 802.11and metropolitan area networks in IEEE 802.16d.

However, OFDM performance is sensitive to receiver synchronization. Frequency offset causes inter-subcarrier interference, and errors in timing synchronization can lead to inter-symbol interference. Therefore, synchronization is critical for good performance in OFDM systems. Much research has focused on improving OFDM synchronization performance and accuracy. Cyclic prefix (CP)-based methods were introduced to determine frequency offset and symbol timing, but do not themselves find the start of a frame. Cyclic Prefix means cyclically extended the guard interval where by each symbol periodic extension of the sequence itself. Since a sequence of known OFDM symbols is embedded into the preamble of each data packet, timing synchronization can be achieved.

1.1. *Correlator*

Generally correlators are also called as multipliers. It *is widely* used in OFDM. In the fourth generation technology there are multiple person passing multiple data or single person passing several information at the same time. So synchronization problem will be occurs. It will overcome we are using correlator. In this correlator mainly used in wireless communication.Correlations are mainly classified as two categories.

(1)Auto correlation: Autocorrelation means using this same signal but different parameter will be used.

(2)Cross correlation: Cross correlation is simply explained as multiplying two different signal with two different parameter.

2. DESIGN OF CORRELATORS

Timing synchronization, resource utilization and power consumption problems of OFDM. In this problem avoiding we are designing correlator. Correlators are simply defined filter. Filter is mainly clearing the output. Correlators are designed we are using preamble symbol. Preamble symbol is using then easily determining output frame sequence value. The downlink preamble in IEEE 802.16d contains two Consecutive OFDM symbols, as shown in Fig. 2.

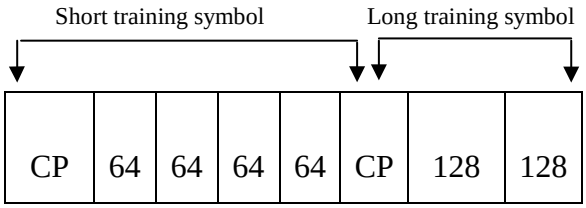

Fig.2 Down link preamble correlator

3. DESIGN OF MULTIPLIER CORRELATORS

This method contains a multiplier followed by a configurable arithmetic unit to provide many independent functions, e.g., multiply, multiply-accumulate, multiply-add, three-input add, and more. It also allows the data path to be configured for various input combinations and register stages; a three stage pipeline offers maximum performance. Since the DSP Slice is designed to mirror the structure of an FIR filter tap, it is ideally suited to implement correlation, and would hence be the method of choice for this application. Our first design uses non-pipelined DSP48E1 Slices in transpose direct form, as shown in Fig.3.1 with 64 coefficients, Pr corresponding to the 64 complex conjugated values of samples in the preamble.

The output of the FIR filter is transpose direct form correlation in it. The coefficients are pre computed according to the IEEE 802.16d standard.

The second design spreads the complex multiply-adds in a five-stage pipeline, shown in the Fig. 3.2.consisting of DSP48E1 Slices configured for three-stage internal pipelining. Ri_ Re and Ri_ Image the real and imaginary parts of received sample, respectively. Pr_ Re and Pr_Im similarly represent the complex conjugation of known preamble .In this existing method diagram is as shown in below Fig 3.1

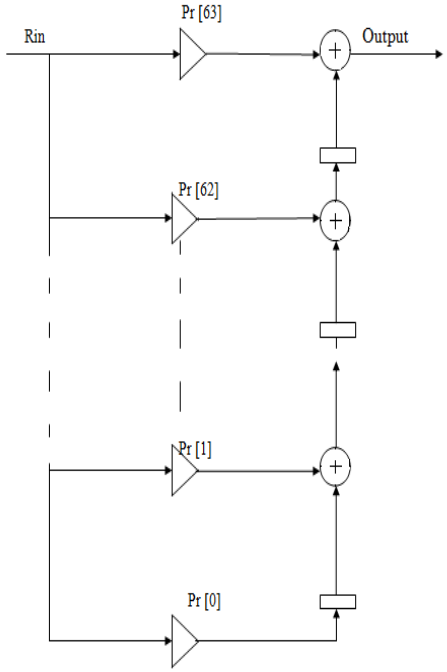

Fig.3.1 Multiplier Correlator

The coefficients are pre computed according to the IEEE 802.16dstandard. The second design spreads the complex multiply-adds in a five-stage pipeline, shown in Fig. 3, consisting of DSP48E1 Slices configured for three-stage internal pipelining. Ri_Re and Ri_Image the real and imaginary parts of received sample, respectively.

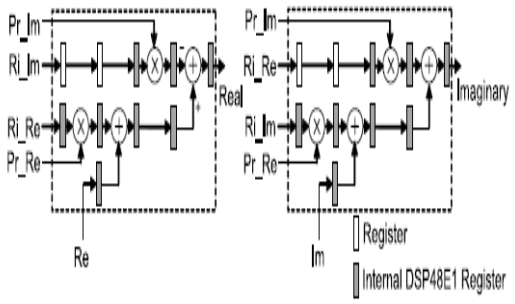

Fig. 3.2 Pipeline structure of the complex number multiply-add.

Fig. 3.2 presents the pipeline structure of the correlator. The additional pipeline registers are required for handling the received sample. Adding pipeline registers should improve the performance significantly .In this pipeline structure of multiplierless correlator is shown in below.

The coefficients are pre computed according to the IEEE 802.16dstandard. The second design spreads the complex multiply-adds in a five-stage pipeline, shown in Fig.3.3, consisting of DSP48E1 Slices configured for three-stage internal pipelining. Ri_Re and Ri_Image the real and imaginary parts of received sample, respectively. In this five stage pipeline structure normally complex multiplication and addition value will be using below structure shown in it.

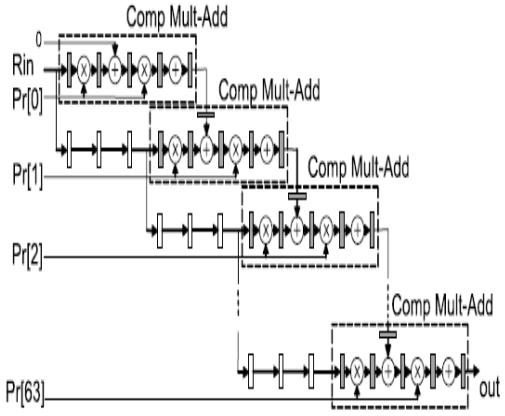

Fig 3.3 Pipeline structure of correlator using DSP48E1 Slices**.**

In above figure of pipeline structure using DSP Slices. Adaptive systems are set to become more main stream, as numerous practical applications in the communications domain emerge. FPGAs offer an ideal implementation platform, combining high performance with flexibility.

While significant research has been undertaken in the area of FPGA partial reconfiguration, it has focused primarily on low-level architecture-specific implementations. Building upon this previous work, we present a system model and software architecture for implementing runtime adaptive applications on FPGA.

4. DESIGN OF MULTIPLIERLESS CORRELATORS USING CARRY LOOK AHEAD ADDER (CLA)

The principle of multiplierlesscorrelators is to represent coefficients and round them in the form of summed powers of 2. Hence, a shift-and-add is performed instead of multiplying by coefficients. It is expected that multiplierless correlation is more efficient, but with embedded hard multipliers in modern FPGAs, it is unclear whether they should still considered favorable. Furthermore, synchronization accuracy must be considered. To explore this, four alternative multiplierless correlators are implemented using four coefficient sets with increasing degrees of rounding, to compare the cost and performance and evaluate against multiplier-based correlators. The coefficient sets are found by quantizing the 64 normalized preamble samples with quantization of 1, 0.5, 0.25, and 0.125.

The proposed structure for multiplierlesscorrelators is shown in figure 4. It shows that timing synchronization for IEEE 802.16a WLANs requires using a correlator to correlate the received signal with a known waveform. Straightforward implementation of this correlator results in the need to perform 320 million complex multiplications per second. This significant requirement can be eliminated by using multiplierlesscorrelators. In this paper, multiplierlesscorrelators are designed based on constraining the real and imaginary parts of correlator coefficients to be sums of powers of two. Sets of coefficients that yield good synchronization performance for simple AWGN channels are first identified; then their goodness for indoor communication environments is verified by simulation for multipath fading channels. Several multiplierlesscorrelators are found the timing synchronization and resource utilization.

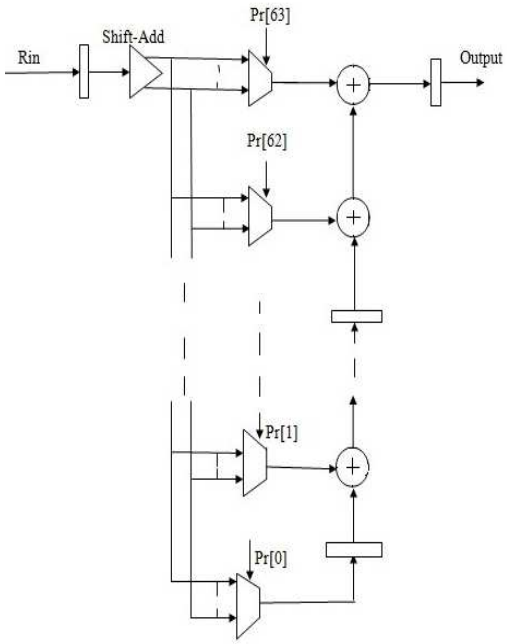

Fig 4 Structure of multiplier less correlator

Comparison among these correlators identifies a good one that requires to perform only 26 addition subtraction operations per correlator output while a similar synchronization performance can be maintained. Correlators that eliminate the need to perform multiplication are designed. Several multiplierless correlators are found. Using this multiplierless correlator leads to considerable reduction in the implementation complexity of receivers. First we are using the data is eight bit data. In this eight bit data is mainly occupy the 0 to 7 bits. Then next in this signal will be passing the Shift_Add block.

Shift_Add block mainly right shift or left shift in it. In this proposed method mainly deals with left shift option .Seven times left shift option will be used. Then next in this value will be passing multiplexer. Multiplexer normally it will act as selected switch. Any value will be choosing at any times. In this section mainly multiplying input coefficients value.

This common Shift_Add block calculates all possible values for 64 coefficients. The multiplexers are used to select the corresponding values from Shift_Add to accumulate in order to generate the correlator output. These are based on the expressed coefficients Pr[n] that are pre computed on the basis of quantizing the 64 preamble samples. Since the Pr[n] values are constants, after synthesizing the design, the multiplexer is optimized .as hard-wired logic, and the preamble cannot be changed.

To support different OFDM preambles, the Pr[n] could be stored in a register, and a real multiplexer used instead of hard-wired logic. This results in increased resource utilization but provides a more flexible solution. Important things in this system we are using Shift Add register. In this register inside inbuilt of the clock in it. In this final output value will be no interference is occurring and timing synchronization will be correctly accurated.

5. Design of Multiplierless Correlators Using Carry Select Adder (CSLA)

Carry select adder is one of the fastest adder used in many data processing processors to perform fast arithmetic function like shift and add operation and so to design resource efficient low power correlator carry select adder is used instead of carry look ahead adder. The design has reduced area, power and resource utilization as compared with the multiplier based correlator. The proposed design of carry select adder is shown in fig 5

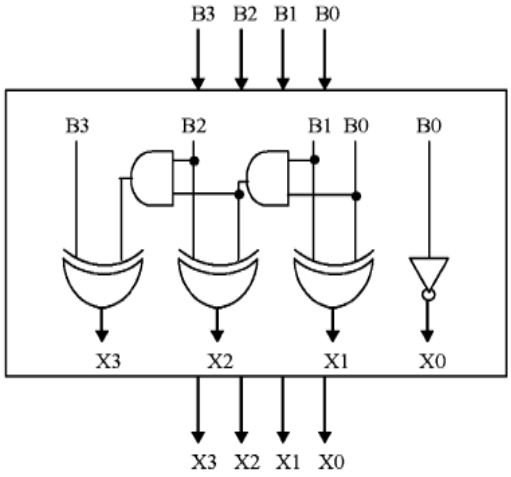

Fig 5.Design of carry select adder

The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. Final stage of this paper multiplierless correlator (CSLA) fit on the adder circuit then determining the power and area.

6. Simulation and Results

In order to validate our designs at the applications level we simulate them using Model Sim with OFDM frame to measure timing synchronization and resource utilization

6.1Simulation for Multiplier Correlator

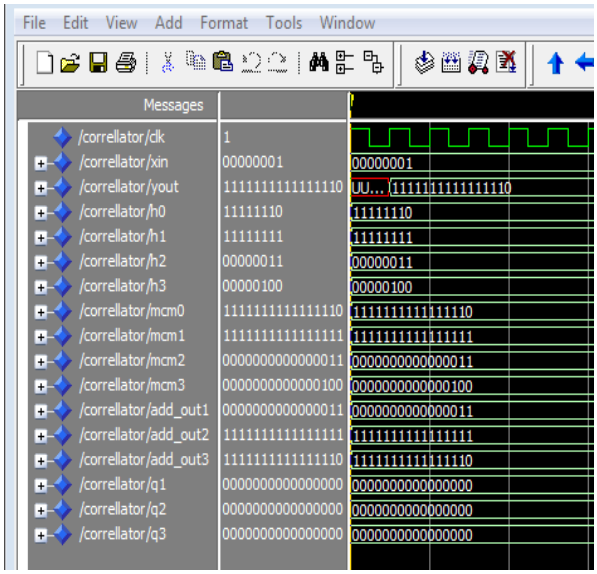

Fig.6.1 Simulation for multiplier correlator

6.1 Simulation for Multiplierless Correlator (CLA)

In this technique first applying the data will be shift 1 or 2 times and original signal should be added in the shifting value. Then the entire shift and add value will be store in the 8:1 multiplexer. Multiplexer is used in selection switch, after selecting the switch we get the corresponding output. In this technique no interference occurs, timing synchronization is measured accurately. So resource utilization will be minimized in this multiplier correlation graph

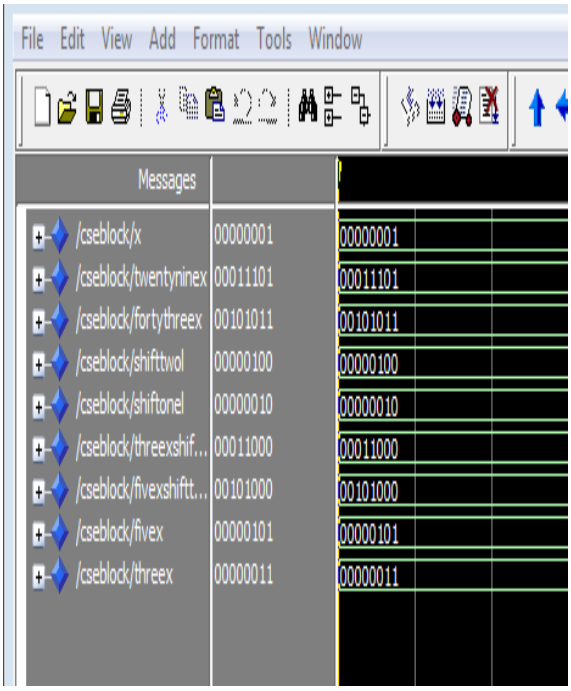

Fig.6 Simulation for multiplier less correlator

Above shows that multiplierless correlator .In this technique first applying the data will be shift 1 or 2 times and original signal should be added in the shifting value. Then all the shift and add value will be store in the 8:1 multiplexer. Multiplexer is used in selection switch, after selecting the switch we get the corresponding output. In this technique no interference occurs, timing synchronization is measured accurately. So resource utilization will be minimized in this multiplier correlation graph.

7. CONCLUSION

The Multiplier normally (DSP Slices) correlators on MODELSIM software seem to offer the ideal resource for simulating correlation-based frame synchronizers. However, as we have discovered, in the context of synchronization for IEEE 802.16 OFDM systems, simplified multiplierless designs offer comparable synchronization performance. While the Multiplier based correlators can obtain higher clock speeds, this is possible only through a detailed pipelined design. Furthermore, their power consumption and resource usage are considerably greater. Since low-power, low-cost devices such as the MODELSIM do not include sufficient DSP Slices, this suggests the adoption of multiplierless designs for low-power implementations in such devices, or whenever only is that it can be used on any FPGA architecture. We have shown that, while very low quantization resolution does impact synchronization performance, with a quantization step size of just 0.5, the synchronization accuracy is on par with multiplier-based correlation. Multiplierless correlation on a Spartan-6 can save over 85% power compared to a DSP Slice .

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